UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,903	10/30/2003	Harm Peter Hofstee	AUS920030403US1	9209

40412 7590 12/30/2005

IBM CORPORATION- AUSTIN (JVL)
C/O VAN LEEUWEN & VAN LEEUWEN
PO BOX 90609
AUSTIN, TX 78709-0609

EXAMINER	
HASSAN, AURANGZEB	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,903	HOFSTEE ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1-7 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/30/2003.

The requirement is still deemed proper and is therefore made FINAL.

2. Applicant's election with traverse of Species II, claims 8-14, 21-27 in the reply filed on 9/27/2005 is acknowledged. The traversal is on the ground(s) that the Species III, claims 15 – 20 are simply computer claims corresponding to the method claims of Species II 8 – 14. This argument is found persuasive by the examiner and Species III 15 – 20 will be examined below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8 – 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushita (US Patent Number 6,366,109).

5. As per claims 8, 15 and 21 Matsushita teaches a method, system and product comprising,

one or more processors (processor, lines 40 – 44);

one or more interface pins (column 1, lines 43 – 45);

a plurality of interface controllers (element 40, figure 1);

a memory accessible by the processors (memory, element 100, figure 4, column 6, lines 18 – 20);

one or more nonvolatile storage devices accessible by the processors; and

an interface pin assignment tool for assigning one or more of the interface pins to one of the interface controllers, the interface pin assignment tool including:

means for receiving a first assignment request (signal, element 44, figure 1);

means for identifying one or more of the interface pins that correspond to the first assignment request (address signal, element 46, figure 2);

means for selecting a first interface controller from the plurality of interface controllers that correspond to the first assignment request (multiplexers, column 6, lines 9 – 23); and

means for associating the identified interface pins with the selected interface controller (recognition decoder, column 6, lines 9 – 23).

6. As per claims 9, 16 and 22 Matsushita teaches a method, system and product wherein the identified interface pins are selected from the group consisting of an input

interface pin (physical pin, column 3, lines 27 – 32) and an output interface pin (outputs, column 7, lines 6 – 12).

7. As per claims 10, 17 and 23 Matsushita teaches a method, system and product comprising,

receiving a second assignment request, the second assignment request corresponding to the identified interface pins (different semiconductor devices, column 6, lines 58 – 67);

selecting a second interface controller from the plurality of interface controllers that correspond to the second assignment request (unit selecting, column 7, lines 56 – 61); and

re-associating the identified interface pins to the second interface controller (column 7, lines 59 – 61).

8. As per claims 11, 18 and 24 Matsushita teaches a method, system and product wherein the associating is performed using a look-up table (pin correspondence table, column 1, lines 26 – 34).

9. As per claims 12, 19 and 25 Matsushita teaches a method, system and product further comprising:

determining whether there are more interface pins that are not associated with the first interface controller (column 6, lines 45 –52); and

assigning the non-associated interface pins to a second interface controller in response to the determination (inactivated, column 6, lines 53 – 57).

10. As per claims 13, 20 and 26 Matsushita teaches a method, system and product comprising,

receiving data from the identified interface pins (input signal); and

providing the data to the first interface controller (input signal, element 62, figure 2, column 4, lines 45 – 49).

11. As per claims 14 and 27 Matsushita teaches a method and product wherein the associating is performed at system initialization.

The process set forth and taught by Matsushita enable it to be performed at system initialization. A method of pin assignment from logical to physical takes place in such an primary stage.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH
12/23/2005

TAMMARA PEYTON
PRIMARY EXAMINER